IN THE CLAIMS

Please cancel claims 1-10, 17-20 and 23-26, without prejudice.

The text of all pending claims, along with their current status, is set forth below:

1-10. (Canceled).

11. (Original) A method for maximizing the use of on-chip cache memory capacity in a chip-multiprocessor, comprising:

forming a two-level cache system with an exclusive cache hierarchy in order to minimize cache line replication and on-chip traffic, the two-level cache system including a first level cache dedicated to each processor in the chip-multiprocessor and a second-level cache shared by all the processors;

associating cache lines with an indication of ownership so that among one or more than one instances of each cache line present in the two-level cache system, there is only one instance that is an owner instance, the indication of ownership being provided only in a second-level cache;

associating the cache lines with state information that includes the indication of ownership, the state information for cache lines present in the first-level cache being maintained in the second-level cache; and

administering cache line ownership and write-backs based on a predetermined guideline.

12. (Original) A method as in claim 11, wherein based the predetermined guideline a first-level cache miss that finds no other copy of a requested cache line becomes an owner of the cache line.

13. (Original) A method as in claim 11, wherein based the predetermined guideline a first-level cache miss that does not find a copy of a cache line in the second-level cache but finds it in one or more than one of the first-level caches receives that cache line from a previous owner and becomes a new owner.

14. (Original) A method as in claim 11, wherein based the predetermined guideline a first-level cache that replaces a cache line, is informed by the second-level cache whether it is owner, in which case it issues a second level cache fill.

15. (Original) A method as in claim 11, wherein based the predetermined guideline whenever the second-level cache has a copy of a cache line, the second-level cache is the owner, and wherein a first-level cache miss that hits in the second-level cache without invalidating it by a write miss does not steal ownership from the second-level cache.

16. (Original) A method as in claim 11, wherein based the predetermined guideline whenever the second-level cache needs to evict a cache line that is additionally present in one or more first-level caches the second-level cache arbitrarily selects one of these first-level caches as the new owner.

17-20. (Canceled).

21. (Original) A two-level cache system in a chip-multiprocessor for maximizing the use of on-chip cache memory capacity in the chip multiprocessor, comprising:

means for forming a two-level cache system with an exclusive cache hierarchy in order to minimize cache line replication and on-chip traffic, the two-level

cache system including a first-level cache dedicated to each processor in the chip-multiprocessor and a second-level cache shared by all the processors;

means for associating cache lines with an indication of ownership so that among one or more than one instances of each cache line present in the two-level cache system, there is only one instance that is an owner instance, the indication of ownership being provided only in a second-level cache;

means for associating the cache lines with state information that includes the indication of ownership, the state information for cache lines present in the first-level cache being maintained in the second-level cache; and

means for administering cache line ownership and write-backs based on a predetermined guideline.

22. (Original) A two-level cache as in claim 21, wherein the system can be implemented in hardware or software or a combination of both.

23-26. (Canceled).